

## CLAIMS

What is claimed is:

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- 1 1. A computer system, comprising:  
2 a processor;  
3 a system memory coupled to said processor; and  
4 an input device coupled to said processor;  
5 said processor having a branch predictor, said branch predictor includes a multi-bank  
6 prediction array, each of said banks comprising a single-ported memory device;  
7 said branch predictor also including bank control logic coupled to said prediction array to  
8 ensure that two accesses to said prediction array in the same cycle do not conflict.
  - 1 2. The computer system of claim 1 wherein said processor further includes fetch logic that  
2 fetches two slots of instructions in one cycle.
  - 1 3. The computer system of claim 1 wherein said branch predictor further includes a  
2 multiplexer coupled to each of said single-ported banks and controlled by said bank control logic.
  - 1 4. The computer system of claim 1 wherein said branch predictor determines an index value  
2 based on a conditional branch instruction and uses said index value to retrieve a prediction from  
3 said prediction array.
  - 1 5. The computer system of claim 4 wherein each of said banks has an identifier and said bank  
2 control logic determines a bank identifier for a conditional branch instruction that is different than

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3 the bank identifier determined for a conditional branch instruction that was last used to access said  
4 prediction array.

1 6. The computer system of claim 4 wherein said bank control logic selects two bits from said  
2 index value to be a bank number.

1 7. The computer system of claim 4 wherein said bank control logic selects two bits from said  
2 index value to be a bank number if the value of said two bits does not equal a bank number  
3 determined for a conditional branch instruction that was last used to access said prediction array.

1 8. The computer system of claim 7 wherein, if said two bits equals said bank number  
2 determined for a conditional branch instruction that was last used to access said prediction array,  
3 then said bank control logic changes the values of said two bits and uses the changed value as a  
4 bank number.

1 9. The computer system of claim 8 wherein said bank control logic changes the value of said  
2 two bits by incrementing the value of said two bits.

1 10. The computer system of claim 3 wherein said branch predictor further includes a pair of 4-  
2 to-1 multiplexers that receive output signals each of said single-ported banks, said pair of  
3 multiplexers are controlled by said bank control logic.

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1 11. The computer system of claim 1 wherein said processor further includes fetch logic that  
2 fetches at least two slots of instructions in one cycle.

1 12. A processor, comprising:  
2 a multi-bank prediction array, each of said banks comprising a single-ported memory  
3 device; and  
4 bank control logic coupled to said prediction array to ensure that two accesses to said  
5 prediction array in the same cycle do not conflict.

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1 13. The processor of claim 12 wherein said processor further includes fetch logic that fetches  
2 two slots of instructions in one cycle.

1 14. The processor of claim 12 wherein said branch predictor further includes a multiplexer  
2 coupled to each of said single-ported banks and controlled by said bank control logic.

1 15. The processor of claim 12 wherein said branch predictor determines an index value based  
2 on a conditional branch instruction and uses said index value to retrieve a prediction from said  
3 prediction array.

1 16. The processor of claim 15 wherein each of said banks has an identifier and said bank  
2 control logic determines a bank identifier for a conditional branch instruction that is different than  
3 the bank identifier determined for a conditional branch instruction that was last used to access said  
4 prediction array.

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1 17. The processor of claim 15 wherein said bank control logic selects two bits from said index  
2 value to be a bank identifier.

1 18. The processor of claim 15 wherein said bank control logic selects two bits from said index  
2 value to be a bank number if the value of said two bits does not equal a bank identifier determined  
3 for a conditional branch instruction that was last used to access said prediction array.

1 19. The processor of claim 18 wherein, if said two bits equals said bank identifier determined  
2 for a conditional branch instruction that was last used to access said prediction array, then said  
3 bank control logic changes the values of said two bits and uses the changed value as a bank  
4 identifier.

1 20. The processor of claim 19 wherein said bank control logic changes the value of said two  
2 bits by incrementing the value of said two bits.

1 21. The processor of claim 14 wherein said branch predictor further includes a pair of 4-to-1  
2 multiplexers that receive output signals each of said single-ported banks, said pair of multiplexers  
3 are controlled by said bank control logic.

1 22. A method of avoiding bank conflicts in a multi-bank prediction array in a processor,  
2 comprising:  
3 generating an index value from a conditional branch instruction address;

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4 selecting two bits from said index value;  
5 comparing the value of said two bits with a previous bank number determined for a  
6 conditional branch instruction previously used to access said prediction array;  
7 using the value of said two bits as a current bank number if said value of said bits differs  
8 from said previous bank number;  
9 if said value of said two bits equals said previous bank number, changing the value of said  
10 two bits to be the current bank number; and  
11 using said current bank number to access the corresponding bank in said prediction array to  
12 retrieve a prediction.

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1 23. The method of claim 22 wherein changing the value of said two bits comprises  
2 incrementing the value of said two bits.